Pin Control and Pin Function Selection (LPC40xx)

Objective

Learn about the selectable features of pins in the LPC40xx MCU, how to enable/disable these features and how to, select a pin's functionality.

Pin Features

The LPC40xx series chips have pins with the following features

see chapter **Chapter 6: LPC408x/407x Pin configuration** & **Chapter 7: LPC408x/407x I/O configuration**

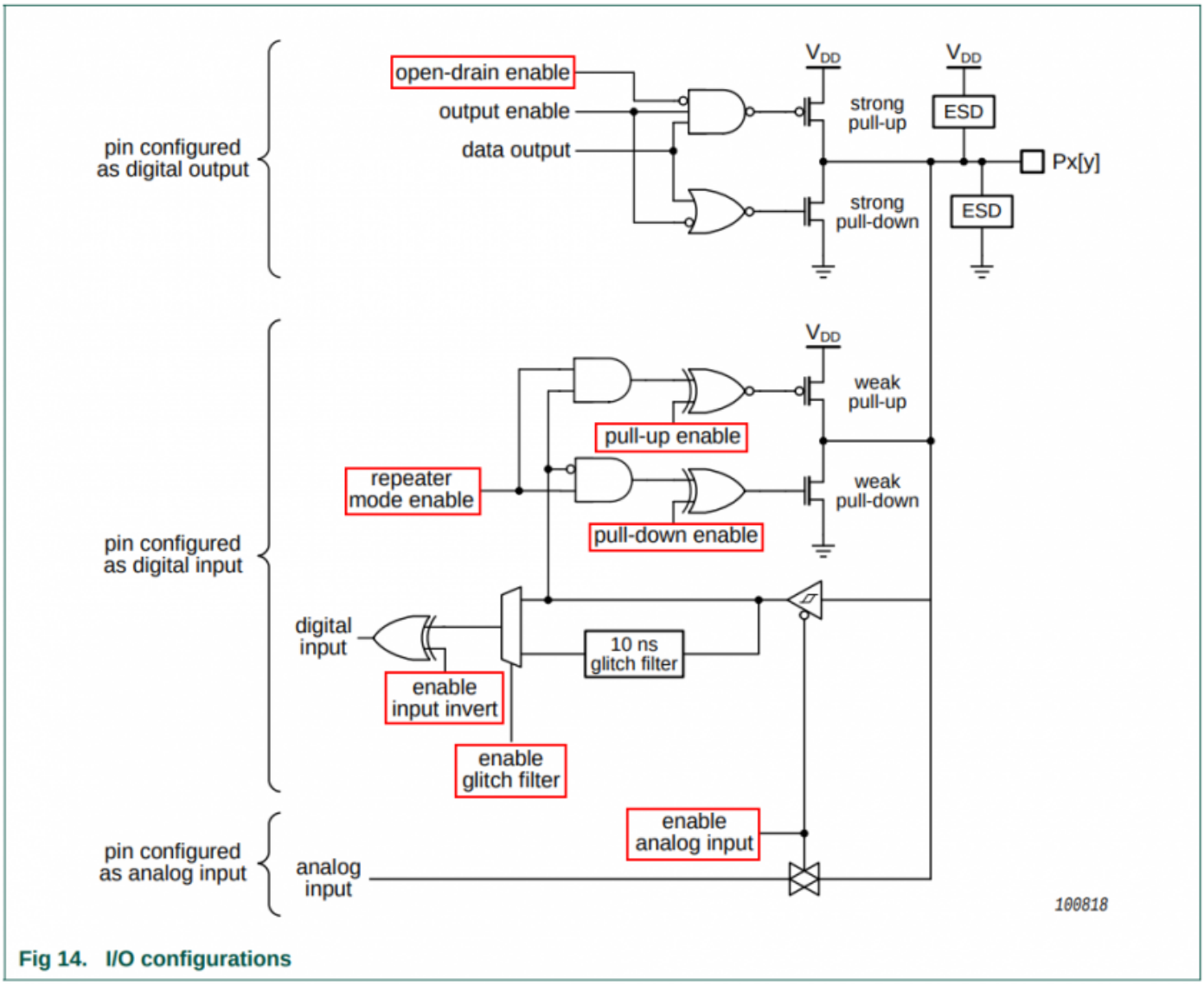

Figure 1. I/O configurations Signals Highlighted (UM10562 LPC40xx Page 122)

- **Open Drain Enable**: Enabling this disables the high side MOSFET in of the totem pole configuration, making that pin an open drain.
- **Pin Modes (Only one or none of these can be active at once)**
  - **Pull-Up Enable**:Enabling this turns on the weak pull-down MOSFET in the ohmic region.
  - **Pull-Down Enable**: Enabling this turns on the weak pull-down MOSFET in the ohmic region.
  - **Repeater Mode Enable**: Enabling this, will activate the pull up or pull down resistor from the last.
- **Enable Input Invert**: Converts a pin configured as an input to active low.
- **Enable Glitch Filter**: Enables the 10nS glitch filter.
- **Enable Analog Input**: Disables schmitt trigger and enables voltage to pass through analog switch to analog input.
- There are actually more controls then this depending on the pin type you are using.

Table 83. Type D IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 84 for specific values.	000
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control). See Section 7.3.2 “Pin mode”.	10
		00	Inactive (no pull-down/pull-up resistor enabled).	
		01	Pull-down resistor enabled.	
		10	Pull-up resistor enabled.	
		11	Repeater mode.	
5	HYS		Hysteresis. See Section 7.3.3 “Hysteresis”.	1
		0	Disable.	
		1	Enable.	
6	INV		Input polarity. See Section 7.3.4 “Input Inversion”.	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
8:7	-		Reserved. Read value is undefined, only zero should be written.	NA
9	SLEW		Driver slew rate. See Section 7.3.7 “Output slew rate”.	0
		0	Standard mode. Output slew rate control is enabled. More outputs can be switched simultaneously.	
		1	Fast mode. Slew rate control is disabled. This mode reduces the output delay by 1 ns compared to the standard mode. Fast mode is recommended for pins used with the EMC, LCD, and SPIFI interfaces.	
10	OD		Controls open-drain mode. See Section 7.3.9 “Open-Drain Mode”.	0
		0	Normal push-pull output	
		1	Simulated open-drain output (high drive disabled)	
31:11	-		Reserved. Read value is undefined, only zero should be written.	NA

Figure 2. Type D IOCON registers (page 132)

Table 85. Type A IOCON registers bit description

Bit	Symbol	Value	Description	Reset value
2:0	FUNC		Selects pin function. See Table 86 for specific values.	0
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control). See Section 7.3.2 “Pin mode”.	10
		00	Inactive (no pull-down/pull-up resistor enabled).	
		01	Pull-down resistor enabled.	
		10	Pull-up resistor enabled.	
		11	Repeater mode.	
5	-		Reserved. Read value is undefined, only zero should be written.	NA
6	INV		Input polarity. See Section 7.3.4 “Input Inversion”.	0
		0	Input is not inverted (a HIGH on the pin reads as 1)	
		1	Input is inverted (a HIGH on the pin reads as 0)	
7	ADMODE		Select Analog/Digital mode. See Section 7.3.5 “Analog/digital mode”.	1
		0	Analog mode.	
		1	Digital mode.	
8	FILTER		Controls glitch filter. See Section 7.3.6 “Input filter”.	1
		0	Noise pulses below approximately 10 ns are filtered out	
		1	No input filtering is done	
9	-		Reserved. Read value is undefined, only zero should be written.	NA
10	OD		Controls open-drain mode. See Section 7.3.9 “Open-Drain Mode”.	0
		0	Normal push-pull output	
		1	Simulated open-drain output (high drive disabled)	
14:11	-		Reserved. Read value is undefined, only zero should be written.	NA
16	DACEN		DAC enable control. This bit applies only to P0[26], which includes the DAC output function DAC_OUT. See Section 7.3.10 “DAC enable”.	0
		0	DAC is disabled	
		1	DAC is enabled	
31:17	-		Reserved. Read value is undefined, only zero should be written.	NA

Figure 3. Type A IOCON registers (page 138)

Table 87. Type U IOCON registers bit description

Bit	Symbol	Description	Reset value
2:0	FUNC	Selects pin function. See Table 88 for specific values.	000
31:3	-	Reserved. Read value is undefined, only zero should be written.	NA

Figure 3. Type U IOCON registers. Only has a function (page 140)

Setting Pin Function

Every GPIO pin of the LPC40xx is capable of other alternative functionalities. Pin selection is the method by which a user is able to designate the functionality of any given pin. For example, GPIO Pin 0.0 can alternatively by used for CAN channel 1 rec[illegible] ata line.

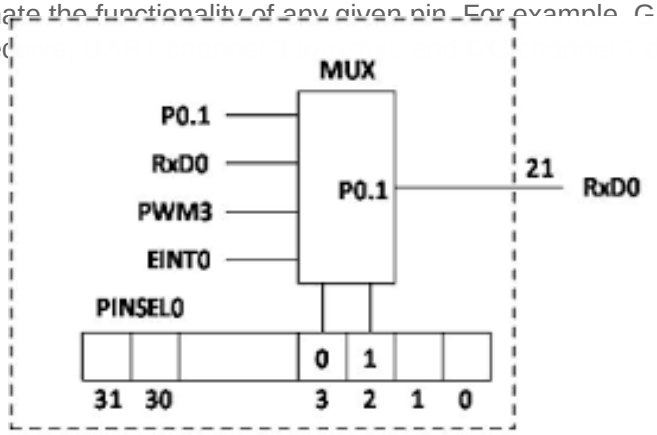

Figure 1B. *I/O Pin Select Mux (from LPC2148, for illustration purposes only)*

```
// Example of setting pin function using LPC40xx.h pointers
// Set as UART 0 Transmit U0_TXD
LPC_IOCON->P0_0 = (LPC_IOCON->P0_0 & ~0b111) | 0b100;
// Set as SSP0_SCKLPC_IOCON->P0_15 = (LPC_IOCON->P0_15 & ~0b111) | 0b010;
```

For example, if one desires to configure pin 0.09 to enable a pull-up resistor and open drain mode, one must clear bits 18 & 19 of PINMODE0 register, and set bit 9 of register PINMODE_OD0.

```
// Using the memory address from the datasheet
*(0x4002C040) &= ~(0x3 << 18);// Clear bits 18 & 19
*(0x4002C068) |= (0x1 << 9);// Set bit 9
// Using LPC17xx.h pointers
LPC_PINCON->PINMODE0 &= ~(0x3 << 18);// Clear bits 18 & 19
LPC_PINCON->PINMODE_OD0 |= (0x1 << 9);// Set bit 9
```

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