

# Pin Selection and Pin Mode

## Objective

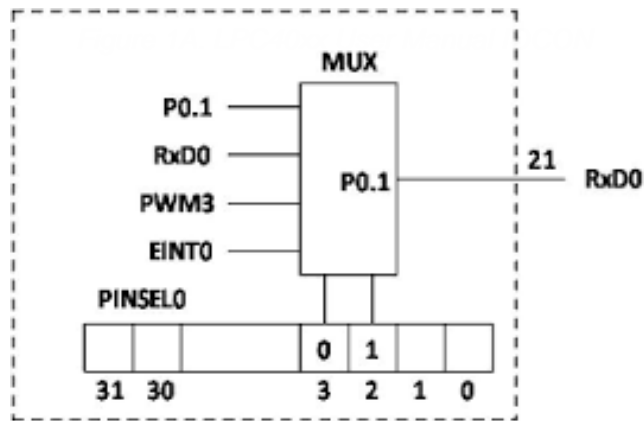
Know how to select a specific functionality of a given LPC40xx pin. Know how to select a pin mode.

## Pin Selection

Every GPIO pin of the LPC40xx is capable of other alternative functionalities. Pin selection is the method by which a user is able to designate the functionality of any given pin. For example, GPIO Pin 0.0 can alternatively be used for CAN channel 1 receive, UART channel 3 transmit, and I2C channel 1 data line.

**Table 84. Type D I/O Control registers: FUNC values and pin functions**

Register	Value of FUNC field in IOCON register							
	000	001	010	011	100	101	110	111
IOCON_P0_0	P0[0]	CAN_RD1	U3_TXD	I2C1_SDA	U0_TXD			
IOCON_P0_1	P0[1]	CAN_TD1	U3_RXD	I2C1_SCL	U0_RXD			
IOCON_P0_2	P0[2]	U0_TXD	U3_TXD					
IOCON_P0_3	P0[3]	U0_RXD	U3_RXD					
IOCON_P0_4	P0[4]	I2S_RX_SCK	CAN_RD2	T2_CAP0		CMP_ROSC		LCD_VD[0]
IOCON_P0_5	P0[5]	I2S_RX_WS	CAN_TD2	T2_CAP1		CMP_RESET		LCD_VD[1]
IOCON_P0_6	P0[6]	I2S_RX_SDA	SSP1_SSEL	T2_MAT0	U1_RTS	CMP_ROSC		LCD_VD[8]
IOCON_P0_10	P0[10]	U2_TXD	I2C2_SDA	T3_MAT0				LCD_VD[5]
IOCON_P0_11	P0[11]	U2_RXD	I2C2_SCL	T3_MAT1				LCD_VD[10]
IOCON_P0_14	P0[14]	USB_HSTEN2	SSP1_SSEL	USB_CONNECT2				
IOCON_P0_15	P0[15]	U1_TXD	SSP0_SCK			SPIFI_IO[2]		
IOCON_P0_16	P0[16]	U1_RXD	SSP0_SSEL			SPIFI_IO[3]		
IOCON_P0_17	P0[17]	U1_CTS	SSP0_MISO			SPIFI_IO[1]		
IOCON_P0_18	P0[18]	U1_DCD	SSP0_MOSI			SPIFI_IO[0]		
IOCON_P0_19	P0[19]	U1_DSR	SD_CLK	I2C1_SDA				LCD_VD[13]
IOCON_P0_20	P0[20]	U1_DTR	SD_CMD	I2C1_SCL				LCD_VD[14]
IOCON_P0_21	P0[21]	U1_RI	SD_PWR	U4_OE	CAN_RD1	U4_SCLK		
IOCON_P0_22	P0[22]	U1_RTS	SD_DAT[0]	U4_TXD	CAN_TD1	SPIFI_CLK		
IOCON_P1_0	P1[0]	ENET_TXD0		T3_CAP1	SSP2_SCK			
IOCON_P1_1	P1[1]	ENET_TXD1		T3_MAT3	SSP2_MOSI			
IOCON_P1_2	P1[2]	ENET_TXD2	SD_CLK	PWM0[1]				
IOCON_P1_3	P1[3]	ENET_TXD3	SD_CMD	PWM0[2]				
IOCON_P1_4	P1[4]	ENET_TX_EN		T3_MAT2	SSP2_MISO			
IOCON_P1_8	P1[8]	ENET_CRS		T3_MAT1	SSP2_SSEL			
IOCON_P1_9	P1[9]	ENET_RXD0		T3_MAT0				
IOCON_P1_10	P1[10]	ENET_RXD1		T3_CAP0				
IOCON_P1_11	P1[11]	ENET_RXD2	SD_DAT[2]	PWM0[6]				
IOCON_P1_12	P1[12]	ENET_RXD3	SD_DAT[3]	PWM0_CAP0		CMP1_OUT		
IOCON_P1_13	P1[13]	ENET_RX_DV						



**Figure 1B.** I/O Pin Select Mux (from LPC2148, for illustration purposes only)

In order to select the I2C2\_SDA functionality of pin 0.10, one must set bit 1, reset bit 0 & 3 of the IOCON register function field to 010.

```
// Using LPC40xx.h pointers
LPC_IOCON->P0_10 &= ~0b010; // reset all bits of function[2:0]
LPC_IOCON->P0_10 |= 0b010; // set the function bit for I2C2
```

## Pin Mode

The LPC17xx has several registers dedicated to setting a pin's mode. Mode refers to enabling/disabling pull up/down resistors as well as open-drain configuration. PINMODE registers allow users to enable a pull-up (00), enable pull up and pull down (01), disable pull up and pull down (10), and enable pull-down (11). PINMODE\_OD registers allow users to enable/disable open-drain mode.

PINMODE0	Pin mode select register 0	R/W	0	0x4002 C040
PINMODE1	Pin mode select register 1	R/W	0	0x4002 C044
PINMODE2	Pin mode select register 2	R/W	0	0x4002 C048
PINMODE3	Pin mode select register 3.	R/W	0	0x4002 C04C
PINMODE4	Pin mode select register 4	R/W	0	0x4002 C050
PINMODE5	Pin mode select register 5	R/W	0	0x4002 C054
PINMODE6	Pin mode select register 6	R/W	0	0x4002 C058
PINMODE7	Pin mode select register 7	R/W	0	0x4002 C05C
PINMODE9	Pin mode select register 9	R/W	0	0x4002 C064
PINMODE_OD0	Open drain mode control register 0	R/W	0	0x4002 C068
PINMODE_OD1	Open drain mode control register 1	R/W	0	0x4002 C06C
PINMODE_OD2	Open drain mode control register 2	R/W	0	0x4002 C070
PINMODE_OD3	Open drain mode control register 3	R/W	0	0x4002 C074
PINMODE_OD4	Open drain mode control register 4	R/W	0	0x4002 C078

**Table 87. Pin Mode select register 0 (PINMODE0 - address 0x4002 C040) bit description**

PINMODE0	Symbol	Value	Description	Reset value
1:0	P0.00MODE		Port 0 pin 0 on-chip pull-up/down resistor control.	00
		00	P0.0 pin has a pull-up resistor enabled.	
		01	P0.0 pin has repeater mode enabled.	
		10	P0.0 pin has neither pull-up nor pull-down.	
		11	P0.0 has a pull-down resistor enabled.	
3:2	P0.01MODE		Port 0 pin 1 control, see P0.00MODE.	00
5:4	P0.02MODE		Port 0 pin 2 control, see P0.00MODE.	00
7:6	P0.03MODE		Port 0 pin 3 control, see P0.00MODE.	00
9:8	P0.04MODE <sup>[1]</sup>		Port 0 pin 4 control, see P0.00MODE.	00
11:10	P0.05MODE <sup>[1]</sup>		Port 0 pin 5 control, see P0.00MODE.	00
13:12	P0.06MODE		Port 0 pin 6 control, see P0.00MODE.	00
15:14	P0.07MODE		Port 0 pin 7 control, see P0.00MODE.	00
17:16	P0.08MODE		Port 0 pin 8 control, see P0.00MODE.	00
19:18	P0.09MODE		Port 0 pin 9control, see P0.00MODE.	00
21:20	P0.10MODE		Port 0 pin 10 control, see P0.00MODE.	00
23:22	P0.11MODE		Port 0 pin 11 control, see P0.00MODE.	00
29:24	-		Reserved.	NA
31:30	P0.15MODE		Port 0 pin 15 control, see P0.00MODE.	00

*Figure 3. LPC17xx User Manual PINMODE0*

**Table 94. Open Drain Pin Mode select register 0 (PINMODE\_OD0 - address 0x4002 C068) bit description**

PINMODE_OD0	Symbol	Value	Description	Reset value
0	P0.00OD <sup>[3]</sup>		Port 0 pin 0 open drain mode control.	0
		0	P0.0 pin is in the normal (not open drain) mode.	
		1	P0.0 pin is in the open drain mode.	
1	P0.01OD <sup>[3]</sup>		Port 0 pin 1 open drain mode control, see P0.00OD	0
2	P0.02OD		Port 0 pin 2 open drain mode control, see P0.00OD	0
3	P0.03OD		Port 0 pin 3 open drain mode control, see P0.00OD	0
4	P0.04OD		Port 0 pin 4 open drain mode control, see P0.00OD	0
5	P0.05OD		Port 0 pin 5 open drain mode control, see P0.00OD	0
6	P0.06OD		Port 0 pin 6 open drain mode control, see P0.00OD	0
7	P0.07OD		Port 0 pin 7 open drain mode control, see P0.00OD	0
8	P0.08OD		Port 0 pin 8 open drain mode control, see P0.00OD	0
9	P0.09OD		Port 0 pin 9 open drain mode control, see P0.00OD	0

*Figure 4. LPC17xx User Manual PINMODE\_OD0*

For example, if one desires to configure pin 0.09 to enable a pull-up resistor and open drain mode, one must clear bits 18 & 19 of PINMODE0 register, and set bit 9 of register PINMODE\_OD0.

```
// Using the memory address from the datasheet
*(0x4002C040) &= ~(0x3 << 18); // Clear bits 18 & 19
*(0x4002C068) |= (0x1 << 9); // Set bit 9
// Using LPC17xx.h pointers
LPC_PINCON->PINMODE0 &= ~(0x3 << 18); // Clear bits 18 & 19
LPC_PINCON->PINMODE_OD0 |= (0x1 << 9); // Set bit 9
```

You may find it helpful to automate register setting and/or clearing. Per our Coding Standards, [inline functions](#) should be used (not Macros).

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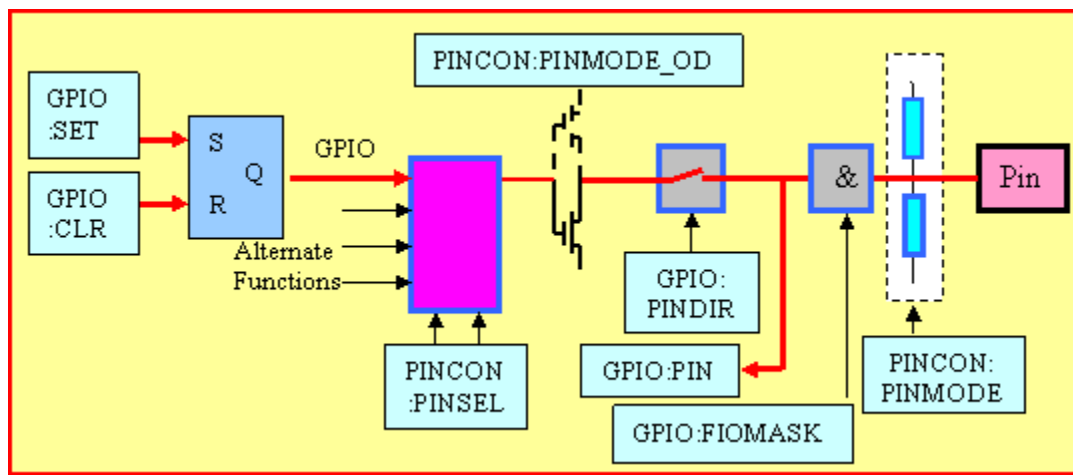


Figure 5. LPC17xx Pin Registers & Circuit (credit: [https://sites.google.com/site/johnkneenmicrocontrollers/input\\_output/io\\_1768](https://sites.google.com/site/johnkneenmicrocontrollers/input_output/io_1768))

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